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10/804,024	03/19/2004	Charles Douglas Murphy		6929

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CHARLES DOUGLAS MURPHY  
601 LINDEN PLACE #210  
EVANSTON, IL 60202

EXAMINER

CHO, JAMES HYONCHOL

ART UNIT	PAPER NUMBER
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2819

DATE MAILED: 05/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/804,024

Applicant(s)

MURPHY, CHARLES DOUGLAS

Examiner

James Cho

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 February 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 2-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 19 and 20 is/are allowed.
- 6) ☒ Claim(s) 2-5 and 7-18 is/are rejected.
- 7) ☒ Claim(s) 6 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

Receipt is acknowledged of the Amendment filed 2-27-2006.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 2-5 and 7-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Laflaquiere et al. (US PAT No. 6,850,176).

Regarding claim 2, Fig. 6 of Laflaquiere et al. teaches a machine for time-to-threshold analog-to-digital conversion in a digital imaging system comprising: a first photodetector (photo-detector 20) having a first photodetector output (output of 20), a threshold detector (comparator 26 detects an input voltage and compared with a threshold voltage; col. 5, lines 23-35) having a first analog input (input coupled to node 35) and a first digital output (output at node  $\beta$ ), the threshold detector comprising: a first transistor (34) having a first gate the first transistor being an n-type MOS transistor (34 is NMOS denoted by the arrow pointing outward), a second transistor (33) having a second gate, the second transistor being a p-type MOS transistor (32 is PMOS denoted by the arrow pointing inward), means for applying the first analog input to the first gate and to the second gate (signal at input node 35 is applied to gates of 33 and 34 via 31

and 32), and means for applying the first photodetector output as the first analog input (30 and 22 provides means for applying output of 20 to the node 35).

Regarding claim 3, Fig. 6 of Laflaquiere et al. teaches the machine of claim 2 in which the first transistor has a first transistor drain and a first transistor source, the second transistor has a second transistor drain and a second transistor source, the first transistor drain and the second transistor source are directly connected (33 and 34 having drain and source respectively are directly coupled in series where the drain of 34 is coupled to the source of 33).

Regarding claim 4, Fig. 6 of Laflaquiere et al. teaches the machine of claim 3 in which the first transistor source is directly connected to a first power supply rail (ground) the second transistor drain is directly connected to a second power supply rail ( $V_r$ ).

Regarding claim 5, Fig. 6 of Laflaquiere et al. teaches the machine of claim 4 in which the first power supply rail has a more negative potential than the second power supply rail (ground is more negative than  $V_r$ ).

Regarding claim 7, Fig. 6 of Laflaquiere et al. teaches a machine for time-to-threshold analog-to-digital conversion in a digital imaging system, comprising: a first photodetector (photo-detector 20) having a first photodetector output (output of 20 applied to node 35 via 30), a threshold detector (comparator 26 detects an input voltage

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and compared with a threshold voltage; col. 5, lines 23-35) having a first analog input (input coupled to node 35) and a first digital output (output at node  $\beta$ ), the threshold detector comprising: a first transistor (34) having a first gate, a second transistor (33) having a second gate, means for applying the first analog input to the first gate and to the second gate (signal at node 35 is applied to the gates of 33 and 34 via 31 and 32), and means for applying the first photodetector output as the first analog input (30 and 22 provides means for applying output of 20 to the node 35) and the threshold detector comprising an inverter (26 has an inverter comprising of transistors 33 and 34).

Regarding claim 8, Fig. 6 of Laflaquiere et al. teaches the machine of claim 7 in which the inverter comprises the first transistor (33) and the second transistor (34).

Regarding claim 9, Fig. 6 of Laflaquiere et al. teaches a machine for time-to-threshold analog-to-digital conversion in a digital imaging system, comprising: a first photodetector (photo-detector 20) having a first photodetector output (output of 20 applied to node 35 via 30), a threshold detector (comparator 26 detects an input voltage and compared with a threshold voltage; col. 5, lines 23-35) having a first analog input (input coupled to node 35) and a first digital output (output at node  $\beta$ ), the threshold detector comprising: a first transistor (34) having a first gate, a second transistor (33) having a second gate, means for applying the first analog input to the first gate and to the second gate (signal at node 35 is applied to the gates of 33 and 34 via 31 and 32), and means for applying the first photodetector output as the first analog input (30 and

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22 provides means for applying output of 20 to the node 35) and the threshold detector comprising a digital logic circuit (transistors 33 and 34 forms an inverter digital logic gate).

Regarding claim 10, Fig. 6 of Laflaquiere et al. teaches the machine of claim 9 in which the digital logic gate comprises the first transistor (33) and the second transistor (34).

Regarding claim 11, Fig. 6 of Laflaquiere et al. teaches a machine for time-to-threshold analog-to-digital conversion in a digital imaging system, comprising: a first photodetector (photo-detector 20) having a first photodetector output (output of 20 applied to node 35 via 30), a threshold detector (comparator 26 detects an input voltage and compared with a threshold voltage; col. 5, lines 23-35) having a first analog input (input coupled to node 35) and a first digital output (output at node  $\beta$ ), the threshold detector being a single-input threshold detector with an implicit threshold level (non-external and implicit threshold voltage defined by intrinsic characteristics of transistors forming the comparator; col. 5, lines 20-23), the threshold detector comprising: a first transistor (34) having a first gate, a second transistor (33) having a second gate, means for applying the first analog input to the first gate and to the second gate (signal at node 35 is applied to the gates of 33 and 34 via 31 and 32), and means for applying the first photodetector output as the first analog (30 and 22 provides means for applying output of 20 to the node 35).

Regarding claim 12, Fig. 6 of Laflaquiere et al. teaches a machine for time-to-threshold analog-to-digital conversion in a digital imaging system, comprising: a first photodetector (photo-detector 20) having a first photodetector output (output of 20 applied to node 35 via 30), a threshold detector (comparator 26 detects an input voltage and compared with a threshold voltage; col. 5, lines 23-35) having a first analog input (input coupled to node 35) and a first digital output (output at node  $\beta$ ), the threshold detector comprising: a first transistor (34) having a first gate, a second transistor (33) having a second gate, means for applying the first analog input to the first gate and to the second gate (signal at node 35 is applied to the gates of 33 and 34 via 31 and 32), and means for applying the first photodetector output as the first analog input (30 and 22 provides means for applying output of 20 to the node 35), in the machine the first transistor and the second transistor being located substantially adjacent to the first photodetector (Fig. 6 is an exemplary PEL, a digital elementary input, located in a column; col. 4, lines 7-14 where the photodetector, 20 is substantially adjacent to 33 and 34 through 33 and 34 and there is no long wires required between as shown in Fig. 6 but coupled to transistors via 31 and 32) whereby long wires connecting the first photodetector, the first transistor, and the second transistor are not required.

Regarding claim 13, Fig. 6 of Laflaquiere et al. teaches a machine for time-to-threshold analog-to-digital conversion in a digital imaging system, comprising: a first photodetector (photo-detector 20) having a first photodetector output (output of 20 applied to node 35 via 30), a threshold detector (comparator 26 detects an input voltage

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and compared with a threshold voltage; col. 5, lines 23-35) having a first analog input (input coupled to node 35) and a first digital output (output at node  $\beta$ ), the threshold detector comprising: a first transistor (34) having a first gate, the first transistor being a minimum-size transistor (34 is minimum-sized compared to a big sized power transistor), a second transistor (33) having a second gate, the second transistor being a minimum-size transistor (33 is minimum-sized compared to a big sized power transistor), means for applying the first analog input to the first gate and to the second gate (signal at node 35 is applied to the gates of 33 and 34 via 31 and 32), and means for applying the first photodetector output as the first analog input (30 and 22 provides means for applying output of 20 to the node 35) whereby the semiconductor chip area occupied by the first transistor and the second transistor is less than would be required for non-minimum-size transistors (it's inherent that the smaller first and second transistors would occupy less chip area compared to bigger sized first and second transistors).

Regarding claim 14, Fig. 6 of Laflaquiere et al. teaches a machine for time-to-threshold analog-to-digital conversion in a digital imaging system, comprising: a multiplicity of threshold detectors (multiple PELs of Fig. 6 are connected in rows and columns by buses; col. 4, lines 7-20 as shown in Fig. 2 where each of PELs has a comparator 26 functioning as a threshold detector), each having an input line connected to the gates of at least two transistors (each detector 26 has two transistors 33 and 34 whose gates are coupled to the input node 35 via 31, 32), a digital output (output at



node  $\beta$ ), a multiplicity of photodetectors (photo-detector 20 in each of PELs) each having a photodetector output (output of 20) provided as input to the input line of one of the multiplicity of threshold detectors (output of 20 is provide to the input of the detector 26 via 30), means for measuring a multiplicity of elapsed times when the digital outputs of the threshold detectors change states (determining the time period between the start of the integration time and the instant when the threshold value is exceeded as shown in Fig. 5 and stated in col. 3, lines 52-64, col. 4, lines 54-58, col. 6, lines 37-42 inherently requires a means for measuring the time elapsed).

Regarding claim 15. Fig. 6 of Laflaquiere et al. teaches the machine of claim 14. in which the threshold detectors are single-input threshold detectors with implicit thresholds (non-external and implicit threshold voltage defined by intrinsic characteristics of transistors forming the comparator; col. 5, lines 20-23).

Regarding claim 16. Fig. 6 of Laflaquiere et al. teaches the machine of claim 14 in which the threshold detectors are digital logic gates (26 has a digital logic inverter comprising transistors 33 and 34).

Regarding claim 17. Fig. 6 of Laflaquiere et al. teaches the machine of claim 14 in which the threshold detectors are inverters (26 has a digital logic inverter comprising transistors 33 and 34).

Regarding claim 18. Fig. 6 of Laflaquiere et al. teaches the machine of claim 17 in which the inverters consist of minimum-size transistors (transistors 33 and 34 are minimum-sized compared to a big sized power transistor),

### ***Response to Arguments***

Applicant's arguments filed 2-27-2006 have been fully considered but they are not persuasive.

In response to applicant's argument that Laflaquiere is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Laflaquiere discloses a device including photo-detectors that converts an analogue signal representing charges resulting from the photo-detection of electromagnetic radiation into a digital signal. Contrary to the applicant's allegations throughout the arguments relating to the flaws, errors, and an invalid claims of Laflaquiere, e.g. unusual language "digital elementary point", the text of claim languages, and incorrect Figure 5., Figs. 3 and 6 of Laflaquiere teaches all limitation of broadly set forth claims of the instant application.

Regarding claims 2-5 and 7-18, the applicant argues that Fig. 6 of Laflaquiere does not show "means for applying said first analog input to said first gate and to said second gate". However the examiner notes that the signal at node 35 is applied to the gates of 33 and 34 through 31 and 32 as shown in Fig. 6. The applicant further argue

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that "the Application specification discusses passing the sensor output directly to the first gate and the second gate of the transistors". However, the examiner notes that "the directly coupled" is not in the claims and that limitations appearing in the specification will not be read into the claims.

Regarding claims 9-11, the applicant argues that Fig. 6 of Laflaquiere is not a single-input threshold detector. The examiner notes that the threshold detector 26 of Laflaquiere is a single-input threshold detector where the signal input is at only the node 35 with a threshold voltage defined by the internal characteristic of the transistors forming the comparator as shown in col. 5, lines 19-23. The examiner further notes that claim 9 has no limitation concerning the single-input threshold detector.

Regarding claim 13, the applicant argues that of Laflaquiere teaches away from having the first and second transistors being of minimum size. However, the examiner notes that "a minimum-size transistor" is inherently smaller than non-minimum-size transistor and it's inherent that the smaller first and second transistors would occupy less chip area compared to bigger sized first and second transistors.

Regarding claim 14, the applicant argues that Fig. 6 of Laflaquiere lacks the limitation of a multiplicity of threshold detectors each having an input line connected to the gates of at least two transistors. However, the examiner notes that Fig. 3 shows that each PEL 10 has a photodetector 20 coupled to the comparator 26 where Fig. 2 shows multiple of 10s coupled in parallel to the bus 12 and Fig. 6 shows the details of 20 and 26.

***Allowable Subject Matter***

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Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 19-20 are allowable over the prior art of record.

The following is a statement of reasons for the indication of allowable subject matter: Although Laflaquiere et al. teaches an A/D converter with a photo-detection photodetector, one of ordinary skill in the art would not have been motivated to modify the teaching of Laflaquiere et al. to further includes, among other things, the specific of the first power supply rail being more negative potential than the second power supply rail (claim 6), and means for recording a first value of the digital elapsed time count on the basis of a change in the digital indicator output signal (claim 19).

### ***Conclusion***

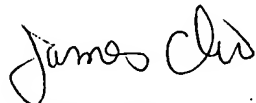
**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492/27492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



James Cho  
Primary Examiner  
Art Unit 2819